TRUETIME

Model 560-5155-1
1, 5, 10 MHz SINE WAVE
FREQUENCY SYNTHESIZER MANUAL

SECTION ONE
1 FUNCTIONAL DESCRIPTION
1.1 PURPOSE OF EQUIPMENT
1.2 PHYSICAL SPECIFICATIONS
1.3 ENVIRONMENTAL SPECIFICATIONS
1.4 POWER REQUIREMENTS
1.5 FUNCTIONAL SPECIFICATIONS
1.5.1 REF A, B, C INPUTS
1.5.2 OUTPUT ACCURACY
1.5.3 SINE WAVE OUTPUTS
1.5.4 DRC CARD COMPATIBILITY
SECTION TWO
2 INSTALLATION AND OPERATION
2.1 HOT SWAPPING
2.2 REMOVAL AND INSTALLATION
2.3 SETUP
2.3.1 560-5155-1 REQUIRED SETTINGS (SW8 & SW9)
2.3.2 PASSIVE COMBINER SELECT SWITCHES (SW3 Through SW7)
2.3.3 INPUT FREQUENCY SELECT SWITCH (SW1)
2.3.4 PLL / BYPASS MODE SELECT SWITCH (SW1)
2.3.5 OUTPUT FREQUENCY SELECT SWITCH (SW2)
2.4 FAULT INDICATIONS
2.4.1 SYNTH FAULT INDICATOR
2.4.2 OUT FAULT INDICATOR
2.4.3 INIT. FAULT INDICATOR
2.4.4 DETAILED FAULT STATUS VIA CPU
SECTION THREE
3 THEORY OF OPERATION
3.1 GENERAL INFORMATION
3.2 HARDWARE DESCRIPTION
3.3 DETAILED DESCRIPTION
3.3.1 PASSIVE COMBINER (Sheet 7)
3.3.2 POWER SUPPLY (Sheet 9)
3.3.3 VOLTAGE CONTROLLED OSCILLATOR (Sheet 6)
3.3.4 FPGA (Sheet 4)
3.3.5 SINE WAVE SHAPERS (Sheet 5)
3.3.6 OUTPUT DRIVERS (Sheet 6)
3.3.7 FAULT DETECTION (Sheets 4, 5, & 8)
3.3.8 BACKPLANE FAULT OUTPUT
3.3.9 FAULT INDICATORS (Sheet 9)
SECTION FOUR
4 DETAILED DRAWINGS
4.1 560-5155 DETAILED DRAWINGS
4.2 560-5155-1 BILL OF MATERIALS

SECTION ONE

1 FUNCTIONAL DESCRIPTION

1.1 PURPOSE OF EQUIPMENT

The TrueTime 560-5155-1 1, 5, 10 MHz Frequency Synthesizer is a plug-in option card for the Model 56000 DRC. This option card offers the user six sine wave outputs at either 1, 5, or 10 MHz (user configurable but one frequency per card at any one time). The outputs provide sine waves at +13 dBm. **As delivered, the outputs are not terminated**. **Each output *must* be terminated into 50 Ω to meet the specifications listed**. Faults may be triggered when connecting or disconnecting the outputs if they are not properly terminated.

The 560-5155-1 Frequency Synthesizer generates an output frequency that is locked to the external reference frequency distributed via REF A, B, or C on the backplane. The reference is received via the passive combiner, which passes only the currently-highest priority reference to the synthesizer. If the currently-highest priority reference is changed, the passive combiner shifts to the next-highest priority input and the synthesizer phase locks to the new reference.

The input frequency that is used to lock the Frequency Synthesizer's PLL (1, 5, or 10 MHz) is switch-selectable. The PLL's oscillator operates at 10 MHz and is the source, in PLL mode for the 1, 5 or 10 MHz signals. The 560-5155-1 card can also operate in Bypass Mode. Bypass Mode means that the signal from the passive combiner's output is the source of the card's outputs, not the on-board PLL / 10 MHz oscillator.

The output frequency is switch-selectable for 1, 5, or 10 MHz. The selected output frequency is output through the backplane connector via six output drivers. The output signals are delivered to external cables via the I/O card installed in the rear slot directly behind the 1, 5, 10 MHz Frequency Synthesizer.

The 560-5155-1 card can operate without a Fault Monitor CPU card installed in the system. In this mode, the 560-5155-1 card offers automatic REF A, B, and C passive combiner operation as previously stated. When the 560-5155-1 card is used in a system that includes the Fault Monitor CPU card, the REF A, B, and C inputs are also controlled by the CPU. When a REF A source's Fault Status is detected (monitored by the CPU), the REF A input on the 560-5155-1 card is disabled. The REF B and REF C inputs are operated similarly -- they are turned off whenever a Fault Status condition for that reference exists. The CPU's REF A, B, and C control feature ensures that only a viable reference oscillator is used on the 560-5155-1 card.

1.2 PHYSICAL SPECIFICATIONS

Dimensions:	0.8"w x 3.94"h x 8.66"d (2 cm x 10 cm x 22 cm)
Weight:	Approximately ½ pound (¼ kg)

1.3 ENVIRONMENTAL SPECIFICATIONS

Operating Temp:	0° to +50°C
Storage Temp:	-40° to +85°C
Humidity:	Up to 95% relative, non-condensing
Cooling Mode:	Convection
Altitude:	Sea level to 10,000 ft.

1.4 POWER REQUIREMENTS

Voltage:	18-72 VDC
Power	4.5 W (all outputs driving 50 Ω @ 1 VRMS)

1.5 FUNCTIONAL SPECIFICATIONS

1.5.1 REF A, B, C INPUTS

Signal Type:	Squarewave or sinewave
Amplitude:	2-5 Vpp
Frequency:	1, 5, or 10 MHz (switch-selectable)

1.5.2 OUTPUT ACCURACY

Long-term:	Equal to reference on REF A, B, or C
Short-term:	Better than 1 part in 10^9 (1 second average)

1.5.3 SINE WAVE OUTPUTS

Quantity:	6
Signal Type:	Analog sinewave
Amplitude:	+13 dBm
Output Impedance:	50 Ω
Harmonic distortion:	-30 dBc
Spurious:	-50 dBc
Phase Noise:	-50 dBc/Hz @ 1 Hz offset -60 dBc/Hz @ 10 Hz offset -95 dBc/Hz @ 100 Hz offset -115 dBc/Hz @ 1 kHz offset -115 dBc/Hz @ 10 kHz offset

1.5.4 DRC CARD COMPATIBILITY

Location:	Slots 1-17 with compatible I/O card in rear slot.
Compatibility:	See Card Compatibility Matrix.

SECTION TWO

2 INSTALLATION AND OPERATION

2.1 HOT SWAPPING

All cards, input cables and output cables are hot swappable. It is not necessary to remove chassis power during insertion or removal. Hot swapping and reference-source changes are abrupt, the effects difficult to characterize; however, the system is designed to protect against permanent effects and minimize temporary effects of these events.

Typically, adjacent-card hot swapping has a negligible effect on the 1, 5, 10 MHz Frequency Synthesizer. Although the hot swapping event directly affects the control voltage of each on-board oscillator, it typically lasts less than one clock-period and has an average of 0 Volts. The effect of redundant power supply switch-over is also negligible.

The effect of a reference-source change is less predictable. The reference frequency is delivered via REF A, B, and C on the backplane. The 1, 5, or 10 MHz Frequency Synthesizer receives the reference via the Passive Combiner. If the currently-highest priority reference is changed, the synthesizer locks to the new reference. When the new reference is in phase with the old reference, the output frequency is affected by less than 1 part in 10^8 over a 1 second period. When the new reference is of opposite phase, the effect can approach 1 part in 10^6. The frequency-shift occurs relatively softly over a 100 ms period, minimizing any effect on downstream equipment. Note that hot swapping a local frequency source, such as an oscillator or fiber optic receiver, qualifies as a hot swap and reference-source change.

The effect of a reference-input perturbation that does not result in a reference-source change (e.g. - removing a cable that is not currently highest priority) at the passive combiner also has an effect on the 1, 5, or 10 MHz Frequency Synthesizer. This is due to the fact that the reference frequency used by the synthesizer is always a weighted sum of REF A, B, and C, and any change has some effect on the resultant waveform. The effect is usually negligible, but can approach 1 part in 10^8.

2.2 REMOVAL AND INSTALLATION

CAUTION: Individual components on this card are sensitive to static discharge. Use proper static discharge procedures during removal and installation.

Refer to CARD COMPATIBILITY section prior to installing new card.

To remove card, loosen the captive retaining hardware at the top and bottom of the assembly, then firmly pull on the handle (or on any connector on rear panel adapter cards) at the bottom of the card. Slide the card free of the frame. Refer to the SETUP section for any required switch settings; or, set them identically to the card being replaced. Reinstall the card in the frame by fitting it into the card guides at the top and bottom of the frame and sliding it in slowly, avoiding contact between bottom side of card and adjacent card front panel, until it mates with the connector. Seat card firmly to avoid contact bounce. Secure the retaining screws at the top and bottom of the card assembly.

2.3 SETUP

The setup of the 560-5155-1 1, 5 or 10 MHz sine wave output card involves selection of the following DIP switches:

1. 560-5155-1 Required Settings (SW8 & SW9)
2. Passive combiner select switches (SW3 through SW7)
3. Input frequency select switch (SW1)
4. PLL / Bypass Mode select switch (SW1)
5. Output frequency select switch (SW2)

2.3.1 560-5155-1 REQUIRED SETTINGS (SW8 & SW9)

SW8 and SW9 must be set as follows:
SW8 switches 1 through 8 = OFF
SW9 switches 1 through 8 = ON

2.3.2 PASSIVE COMBINER SELECT SWITCHES (SW3 through SW7)

Set SW3 through SW7 to match the input frequency in use -- REF A, B, and C frequency reference:

PASSIVE	10 MHz	5 MHz	1 MHz
SW3-1 thru SW7-1	ON	OFF	OFF
SW3-2 thru SW7-2	OFF	ON	OFF
SW3-3 thru SW7-3	OFF	OFF	ON
SW3-4 thru SW7-4	OFF	OFF	OFF

2.3.3 INPUT FREQUENCY SELECT SWITCH (SW1)

Set SW1 to select the proper input frequency. This selection sets FPGA U4 for the proper divide ratio (for the PLL's phase detector).

INPUT	10 MHz	5 MHz	1 MHz
SW1-1	ON	OFF	OFF
SW1-2	OFF	ON	OFF
SW1-3	OFF	OFF	ON

OPERATING MODE	PLL	BYPASS
SW1-4	OFF	ON

2.3.4 PLL / BYPASS MODE SELECT SWITCH (SW1)

Set SW1 switch 4 for the operating mode of choice. NOTE: When the operating mode is Bypass, SYNTH fault reporting (PLL lock) will be suppressed.

2.3.5 OUTPUT FREQUENCY SELECT SWITCH (SW2)

Set SW2 to select the desired output frequency. This selection enables the appropriate sine wave shaping circuit.

OUTPUT	10 MHz	5 MHz	1 MHz
SW2-1	ON	OFF	OFF
SW2-2	OFF	ON	OFF
SW2-3	OFF	OFF	ON

2.4 FAULT INDICATIONS

All indicators activate briefly following hot-insertion or power-up. The following paragraphs describe operation during steady-state conditions.

2.4.1 SYNTH FAULT INDICATOR

The Synthesizer Fault indicator may flash briefly during hot swapping and at the addition or removal of REF A, B, or C. This is a normal condition which occurs as the Voltage Controlled Oscillator (VCO) experiences a reference perturbation (see HOT SWAPPING section for a discussion of the effects of hot swapping).

A continuously-flashing indication shows a phase-locked loop out-of-lock condition. This could be caused by:

1) Input reference off-frequency.
2) Loss of reference on REF A, B, and C. When all references are lost, the VCO will drift to one end of the control range, which is detected as a SYNTH FAULT.
3) Failure of a VCO.

A solid ON SYNTH LED indicates a local power supply failure.

2.4.2 OUT FAULT INDICATOR

The OUT A through OUT F Fault indicators activate when the associated drivers have failed. Note that the detector is designed to detect failed drivers and, typically, will not detect a shorted output.

2.4.3 INIT. FAULT INDICATOR

This is an on-card fault indicator which is not externally visible; although it can be seen by installing the card next to an empty slot. It indicates a failure of the card to initialize properly during power-up. Activation of this LED is accompanied by activation of all of the front panel indicators. Occasionally, this fault is caused by a temporary condition related to the cycling of power and can be cleared by a power or hot swap cycle. If this is unsuccessful, the card is defective.

2.4.4 DETAILED STATUS VIA CPU

The Fault Monitor CPU has access to detailed 560-5155-1 card status. When the CPU card provides the verbose mode serial report, fault status is available in a 2-byte format, with each binary nibble displayed as a hexadecimal (HEX) character.

The Verbose report displays the Fault status. In this context, a reported fault indicates a problem. The Machine report, when used, reports the current status (settings) of the switches and faults in hexadecimal characters. Together, they pinpoint problems and help the technician view the switch settings on the cards.

2.4.5 VERBOSE REPORTS

The following is an example of a Fault Monitor CPU report in Verbose mode:

```
TrueTime 56000 Site 01
Automatic Reports Enabled
Periodic Reports Disabled
Primary Inputs Selected REFA No REFB No REFC Off PRI OK SEC OK TER Off

1. Undefined          OK              Undefined       OK
2. Undefined          OK              Undefined       OK
3. 5155-1       LOCAL OSC FAULT 0047 Undefined OK
4. Undefined          OK              Undefined       OK
```

The above sample tells you that:
Automatic reports are enabled and Periodic reports are disabled.
Primary inputs REF A and REF B are not bussing Aux. Ref. REF C is off.
Primary and Secondary status inputs OK, Tertiary is OFF.

Numbers 1-4 are slots (not all slots are shown in the example). Slots 1,2,and 4 are undefined (empty) and functional (OK).

Slot 3 is read as follows:
5155-1 is the abbreviation of the 560-5155-1 card. The fault reading is 0047.

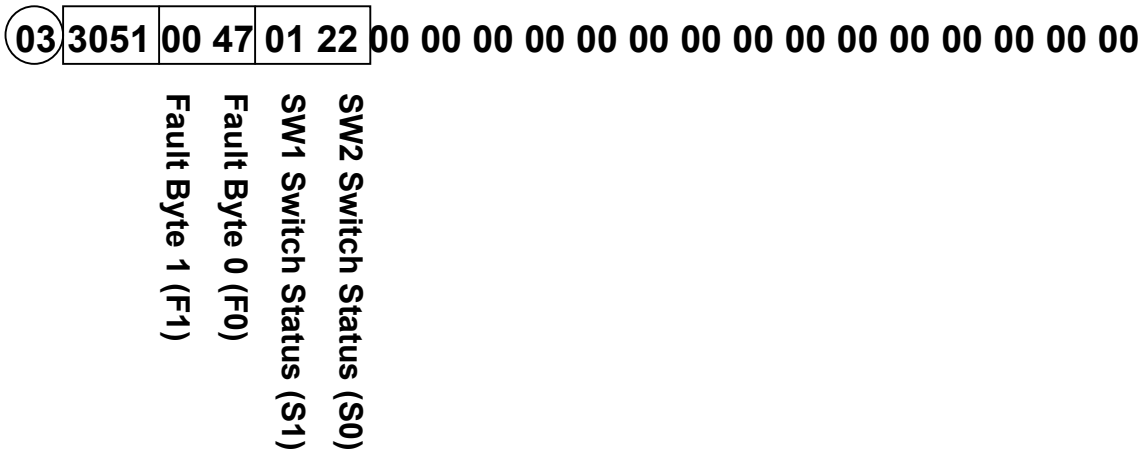
2.4.6 MACHINE REPORTS

The Fault Monitor CPU has another serial output mode called machine report mode. This mode is usually used with a computer program to interrogate the 56000 system status.
The machine report mode displays hexadecimal (HEX) characters like the verbose mode report. (

The following is an example of a Fault Monitor CPU report in Machine Mode:

TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 30 51 00 47 0122 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)

Example from card slot 3 above:

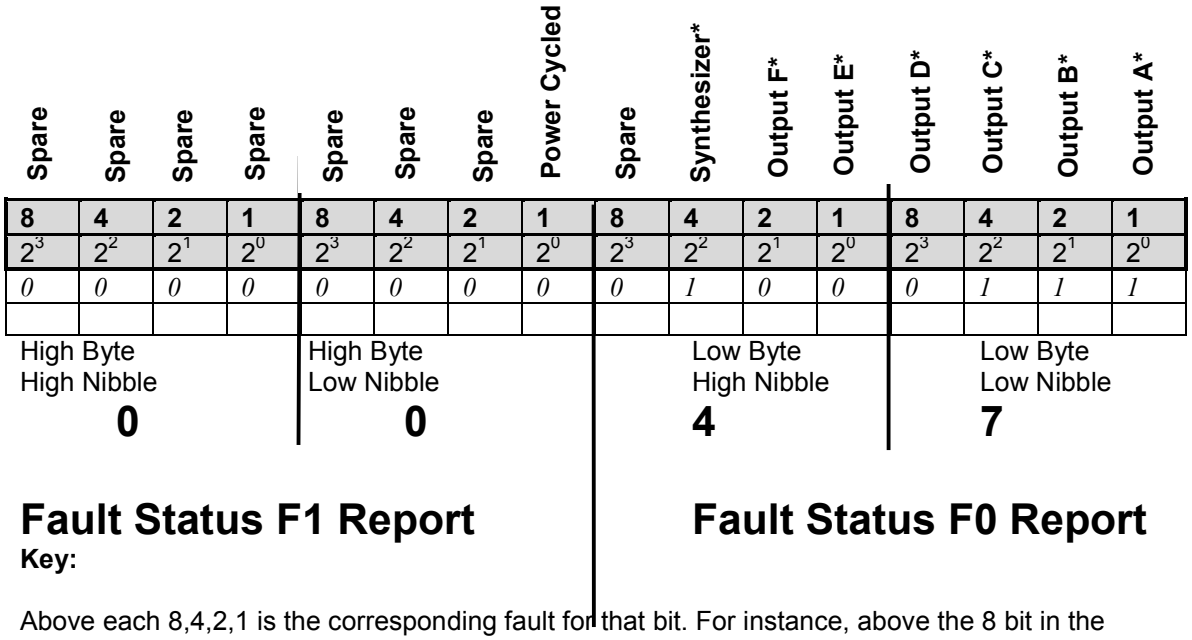


Slot 3 shows that the Fault status is 0047 (F1, F0). The Status report read-out is 0122(S1,S0).

2.4.7 REPORT CONVERSIONS

This section deals with how to read and convert the Fault and Status read-outs using various tables and binary conversions. To decipher a Fault Status report, use Fig. A.
For Status reports (S1, S0) use Fig. B.

Fig. A



Key:

Above each 8,4,2,1 is the corresponding fault for that bit. For instance, above the 8 bit in the Upper byte/Low nibble reads Rub. Lockmon, which is the fault .

* = Latched Fault Bit (Reset via Fault Monitor CPU)

Shaded area

Informational only. The upper row: Bit value hex weights (8,4,2,1) The Lower row corresponds to the hex weight above. For instance, a readout of 7 equals 111 in binary and 4+2+1 hex weight.

Each section of 8,4,2,1 is a nibble of either an Upper or Lower byte and separated for easy recognition. Each nibble = 4 bits and each byte = 8 bits. "00" is the F1 report, "47" the F0 report.

Non-shaded area

This area is used according with the report read-out after a report is converted to binary. The 0407 is an example from a report.

Always read the report from Upper (High) byte to Lower (Low) Byte.

Status (S1, S0) Conversion Table **FIG. B**

STATUS REG 0	Bit	Bit Value	Switch	
Low	0	1	10 MHz Output	
Nibble	1	2	5 MHz Output	**2**
Low	2	4	1 MHz Output	
Byte	3	8	Not Defined	
High	4	1	10 MHz Input	
Nibble	5	2	5 MHz Input	
Low	6	4	1 MHz Input	**2**
Nibble	7	8	Bypass Mode ON	
STATUS REG 1				
Low	0	1	Always 1 (Analog)	
Nibble	1	2	Always 0	
High	2	4	Not Defined	**1**
Byte	3	8	Not Defined	
High	4	1	Not Defined	
Nibble	5	2	Not Defined	
High	6	4	Not Defined	**0**
Byte	7	8	Not Defined	

Notes: The settings listed under the Switch column are HIGH or ON. For instance, frequency has SW 1-1 and SW 1-2. If SW 1-1 is ON, SW 1-2 is presumed to be OFF (although there is no specific mention of this). For switches, a 1 = ON, 0 = OFF.

Example: Graphically, the switch settings look like this:

Switch/Position	10 MHz	5 MHz	1 MHz
1 1	1 (On)	0 (Off)	1 (On)
1 2	0 (Off)	1 (On)	1 (On)

Read from top to bottom for each MHz.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary

0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault/Switch On
0 = No Fault/Switch Off

Use the Binary Conversion table to convert a read-out from the monitor to binary. For instance, if the report read-out was 3C15, this would be:

11\1100\1\101 in binary.

USING THE FAULT STATUS REPORT (F0,F1)

The hex weight (fault importance) has been assigned 8, 4, 2, 1. Beneath each number is the corresponding fault. Use Fig. A. The report example read 0047. The 0 is high byte/high nibble, the 4, low byte/high nibble, and 7, low byte/low nibble. Each nibble falls under a section on Fig. A., high to low or left to right.

Look at Fig. A. Below this chart is a sample read-out (0047). This read-out would appear on the monitor when a Verbose report is requested. In the example, there are no faults in the high byte/high nibble or in the high byte/low nibble because both are zero (0). In the low byte/high nibble, a 4 is reported. Looking directly above this, a 4 bit is easily spotted. The fault is synthesizor. However, In the low byte/low nibble, a 7 is reported. There is no 7 listed, only a 1, 2, 4, 8. Use the Binary Conversion table to determine the faults.

Seven (7) is converted to 111 in Binary. In Binary, a 1 = fault and 0 = no fault. Read 111 from bottom (low bit) to top (high bit) using the lower byte/low nibble group. The first three (from low bit to high bit) are 1's, indicating there is a fault with the Output Faults A, B and C.

Note that the hex weight assigned totals to 7 (4+2+1). If the 7 had been a 6, in binary this is 110. Reading from low bit to high bit, the 1's (i.e., faults) fall under hex weight 4 and 2, which equals a hex weight of 6. Of course, glancing at the lower byte/low nibble, you can quickly see (without converting to binary) that under 4 and 2 (i.e., 6) are the Output Faults B and C that are in fault.

Each of the four nibbles is grouped by category for easy visual identification of an offending fault. Each nibble has 15 possible fault combinations. All faults are asserted as a logic 1. The faults are latched on the Oscillator card and must be cleared by the 560-5179-1 Fault Monitor CPU “CL” command.

USING THE STATUS REPORT (S1, S0)

The method used for reading the Fault report is the same when reading the Status report. Refer to Fig. B.

Using the same read-out, 0122, but because the table is different, the 0 is located at the bottom (high byte). The rest of the numbers follow upward towards the low byte (Status 0). In this case, the 1 falls in the low nibble\high byte section of Status 1. The 2's fall in the high nibble\ low byte and low nibble\low byte section of Status 0. Two can be converted to 10 in binary.

1 = Active, a 0 = Not active.

The following are active in the Status report.

In Status 1, the readout is 1. The 1 is listed in the Bit Value column in that section, low nibble\high byte , indicating Analog is active.

The first 2, in the Status 0, high nibble\low nibble section, the 5 MHz is active:

10 MHz Output	0
5 MHz Output	1
1 MHz Output	0

The last 2, in Status 0, low nibble\low byte section, the 5 MHz is also active:

10 MHz Input	0
5 MHz Input	1
1 MHz Input	0

QUICK REFERENCE SHEET FOR READING FAULT AND STATUS REPORTS

1. Run a report. This is a portion of a sample Machine report.

TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 30 51 00 47 0122 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)

0047 is the Fault Status read-out
0122 is the Status read-out report

03 3051 00 47 0122 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Fault Byte 1 (F1)
Fault Byte 0 (F0)
SW1 Switch Status (S1)
SW2 Switch Status (S0)

Slot 3 shows that the Fau ıs is 0047 (F1, F0). The Status report read-out is 0122(S1,S0).

00 = Fault Status 1 (F1) report
47 = Fault Status 0 (F0) report
01 = Status 1 (S1) report
22 = Status 0 (S0) report

What's in a number?

0 4 0 7

High Byte High Nibble — High Byte Low Nibble — Low Byte High Nibble — Low Byte Low Nibble

2. When required, convert Decimal to Binary using the Binary Conversion Table.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault/On/Active/Yin
0 = No Fault/Off/Not Active/Yang

SECTION THREE

3 THEORY OF OPERATION

3.1 GENERAL INFORMATION

This section contains a detailed description of the circuits in the 1, 5, 10 MHz Frequency Synthesizer card. Use these descriptions in conjunction with the drawings in SECTION FOUR.

3.2 HARDWARE DESCRIPTION

The 1, 5, 10 MHz Frequency Synthesizer incorporates a Passive Combiner, a DC-to-DC Converter, a phase-locked VCO, three sine wave shaping circuits, six 50 ohm analog output driver, fault-detection circuitry and 7 Fault Indicators.

3.3 DETAILED DESCRIPTION (Reference Drawing 560-5155)

3.3.1 PASSIVE COMBINER (Sheet 7)

The passive combiner is a circuit that strives to always output the desired signal, derived from the three separate inputs REF A, B, and C (named FREQA, B, and C on the schematic), without introducing any switching transient or glitch when one or two of the inputs are lost. It is composed of three input filter sections, three high speed comparators, a weighting network and a passive combining network. The filters and the combining network employ tuned circuits and therefore have to have their values adjusted depending on the required input frequency of either 1, 5, or 10 MHz. This is accomplished by the use of SW3 through SW7, which are 4PST DIP switches. The input filters and the comparators serve to produce a very clean square wave with very good symmetry. These square waves are then buffered and applied to the weighting network where they are summed with different weights in order to give the primary source the greatest influence on the final result. This summing results from an interaction between the weighting network and the combining network which is composed of a parallel resonant tank and a series resonant tank. These tanks are tuned slightly off center to lower the Q so that amplitude variations are minimized when input signals are changed. The final output voltage is then buffered and squared up to produce the final signal called FREQIN.

3.3.2 POWER SUPPLY (Sheet 9)

The DC-to-DC Converter converts 48 VDC backplane power to local ±5 VDC power. It is fully-isolated from the backplane power and referenced to signal GND on the Synthesizer card. Backplane power is supplied via a Polyswitch fuse device, diode and Pi-section L-C filter. The poly-fuse protects the backplane power bus from internal DC-to-DC shorts. The diode and L-C filter serve a triple purpose. During live-insertion, the high-current inductor minimizes in-rush current to the DC-to-DC being inserted; and, the diode and capacitor serve to hold up the local voltage at the input to each currently-installed DC-to-DC. During steady-state conditions, the L-C filter minimizes switching noise coupled back into the backplane power bus. During live-extraction, the 0.1 uF capacitor absorbs the inductive-kick of the opened circuit, minimizing contact-arcing. The -5 VDC side of the supply is artificially loaded,

providing a minimum load to improve output voltage regulation. The power-up reset generator, assures that RESET is active while the +5 VDC supply is between 1 and 4.5 VDC. This guarantees proper configuration of the Xilinx FPGA during hot swapping and power-up.

3.3.3 VOLTAGE CONTROLLED OSCILLATOR (Sheet 6)

The card is equipped with a 10 MHz VCO. This VCO is locked to a 1 MHz reference frequency (derived from REF A, B, or C) via a phase-comparator located within the Xilinx FPGA. The filtered phase comparison output from the PLL's integrator is connected to the voltage control input of the 10 MHz oscillator, closing the loop. The 10 MHz output from the on-board oscillator is the clock source for the 1, 5, or 10 MHz output when the card is set for PLL Mode.

3.3.4 FPGA (Sheet 4)

The Field Programmable Gate Array (FPGA) is the interface between the 1, 5, 10 MHz frequency synthesizer card and the CPU (if installed). The FPGA provides the timing and control signals for the synthesizer card in both stand-alone and CPU operating modes.

3.3.5 SINE WAVE SHAPERS (Sheet 5)

The XMPPS signal from the FPGA connects to three ACMOS AND gates. This signal is either 1, 5, or 10 MPPS depending on the setting of SW2 the Output Frequency select switch. In PLL Mode, the XMPPS signal is derived from the on-board 10 MHz oscillator. In the Bypass Mode, the XMPPS frequency rate is the signal that gets through the passive combiner circuit, therefore, the SW2 settings must match the input frequency in this mode.

NOTE: The passive combiner filter is not as sharp as the sine wave shaper filter. The passive combiner output (FREQIN) can pass a signal to the XMPPS output that is far enough off frequency that the sine wave shaper and thus output amplitude from the card can be lower than the specified +13 dBm.

Only one sine wave shaper is enabled at a time. The selected output frequency, derived from the SW2 setting, enables the appropriate sine wave shaper circuit. The selected AND gate drives a series LC and a parallel LC filter to produce the sine wave. The output from each of the sine wave filters connect to output level control pots. These pots have been factory set to provide sine wave outputs at +13 dBm. The pots connect to an analog switch which outputs the selected frequency sine wave to a fixed gain amplifier.

3.3.6 OUTPUT DRIVERS (Sheet 6)

The sine wave output from the fixed gain amplifier connects to six analog 50 ohm buffers. These buffers are connected through analog output switch SW9 to the backplane connector P1. NOTE: SW9 is factory set all ON, SW8 all OFF.

3.3.7 FAULT DETECTION (Sheets 4, 5 & 8)

There are two categories of fault detection: Output Driver faults and synthesizer faults. Both use a combination of discrete components and Xilinx FPGA logic to perform the detection task.

The monitored signal outputs on the 560-5155-1 card are DRIVOUT A through DRIVOUT F. The DRIVOUT signals connect to the output driver fault detectors which consists of 6 peak detectors and 6 voltage comparators. The voltage comparator outputs provide a logic low when the associated output is OK and a logic high when the output is bad. The comparator outputs are connected to the FGPA which recognizes the logic level, activates the appropriate fault status indicator and reports the DRIVOUT failure to the CPU card.

The 1, 5, or 10 MHz frequency synthesizer (SYNTH FAULT) detector utilizes four voltage comparators to detect an out-of-lock condition in the 10 MHz VCO. These comparators verify that the VCO control voltage and filtered phase comparator voltage are within defined limits. If the control voltage is out of tolerance, circuitry in the FPGA is activated.

3.3.8 BACKPLANE FAULT OUTPUT

Inside the FPGA, all faults are combined to form a composite fault signal which is used to drive the Fault line to the Fault Monitor CPU. Fault-signal active indicates status-bit true. (Note that the FAULT signal is active-low on the backplane.) Refer to manual section 2.4.4 for detailed information on the fault reporting.

3.3.9 FAULT INDICATORS (Sheet 9)

The INIT. FAULT indicator is driven by the FPGA Initialization-done signal. It activates during initialization, and remains active if initialization does not complete. This is an extremely unusual occurrence.

The SYNTH. FAULT indicator is powered directly from the backplane 48 VDC power buss and is controlled via an opto-isolator to maintain 48 VDC isolation. If local 5 VDC power is lost, the SYNTH. FAULT indicator will be ON. The indicator is held off by the fault detection logic while the 10 MHz VCO is functioning within limits. When the 10 MHz VCO is locked, the indicator will be OFF. When the 10 MHz VCO is not locked, the SYNTH. FAULT indicator will blink ON and OFF.

The OUT fault indicators are controlled directly by the fault detection logic.

SECTION FOUR

4. DETAILED DRAWINGS

4.1	560-5155	DETAILED DRAWINGS
4.2	560-5155-1	BILL OF MATERIALS